UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/484,549	01/18/2000	Korbin Van Dyke	01000.9901080	9816

29153 7590 10/19/2005

ATI TECHNOLOGIES, INC.
C/O VEDDER PRICE KAUFMAN & KAMMHOLZ, P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
ALI, SYED J	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/484,549	DYKE ET AL.	
	Examiner	Art Unit	
	Syed J. Ali	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed August 5, 2005. Claims 2-12 and 14-17 are presented for examination.

2. The text of those sections of Title 35, U.S. code not included in this office action can be found in a prior office action.

Claim Rejections - 35 USC § 102

3. **Claims 2-12 and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Bonola (USPN 5,706,514).**

4. As per claim 15, Bonola teaches the invention as claimed, including a method for providing multimedia functionality in a homogeneous multiprocessor environment comprising:

queuing tasks (col. 3 lines 61-65);

identifying available processing resources in the homogeneous multiprocessor environment (col. 7 lines 36-38);

allocating the available processing resources among the tasks based on the capabilities of each of the available processing resources and the processing requirements of each of the tasks (col. 7 lines 42-52; col. 8 lines 11-13);

providing to the available processing resources functional programs and initial data corresponding to the tasks (col. 8 lines 13-18); and

performing the tasks using the available processing resources to produce resulting data (col. 9 lines 13-23), wherein the functional programs cause the available processing resources to perform the tasks of at least one of: graphics image processing, video processing, audio processing and communications processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

5. As per claim 2, Bonola teaches the invention as claimed, including the method of claim 15 wherein a plurality of processors of the homogeneous multiprocessor environment are capable of executing a first instruction of a first instruction set and a second instruction of a second instruction set (col. 2 lines 6-10; col. 3 lines 37-44).

6. As per claim 3, Bonola teaches the invention as claimed, including the method of claim 2 wherein the first instruction and the second instruction share an identical bit pattern but perform different operations (col. 1 lines 15-26).

7. As per claim 4, Bonola teaches the invention as claimed, including the method of claim 3 wherein a first processor of the plurality of processors executes an input/output kernel program, the input/output kernel program including a first portion expressed using the first instruction set and a second portion expressed using the second instruction set (col. 3 lines 26-35; col. 7 lines 22-33).

8. As per claim 5, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

converting a functional program of the functional programs expressed using the first instruction set to an equivalent functional program expressed using the second instruction set (col. 8 lines 31-45).

9. As per claim 6, Bonola teaches the invention as claimed, including the method of claim 3 wherein the tasks comprise x86 processing (col. 1 lines 15-26, wherein graphic image processing, video processing, audio processing, and communication processing are just some of the types of tasks that can be performed on an x86 system).

10. As per claim 7, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

receiving the initial data from a first input/output device (col. 8 lines 11-15).

11. As per claim 8, Bonola teaches the invention as claimed, including the method of claim 3 further comprising the step of:

passing the resulting data to a first input/output device (col. 9 lines 13-23).

12. As per claim 9, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to the first input/output device further comprises the step of:

passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device (col. 9 lines 13-23).

13. As per claim 10, Bonola teaches the invention as claimed, including the method of claim 9 wherein the step of passing the resulting data through an intermediary device, wherein the intermediary device is coupled to the first input/output device and to a second input/output device further comprises the step of:

automatically adapting to a reallocation of the available processing resources among the tasks (col. 8 lines 46-65).

14. As per claim 11, Bonola teaches the invention as claimed, including the method of claim 8 wherein the step of passing the resulting data to a first input/output device further comprises the step of:

passing the resulting data to a mixed-signal device (col. 9 13-15, 19-23).

15. As per claim 12, Bonola teaches the invention as claimed, including the method of claim 3 wherein the step of allocating the available processing resources among the tasks is dynamically adjusted (col. 8 lines 46-65).

16. As per claim 16, Bonola teaches the invention as claimed, including the method of claim 15, further comprising:

keeping track, remotely from the resources, of the capabilities of all available processing resources (col. 7 lines 42-52); and

identifying available processing resources in the homogeneous multiprocessor environment based solely on the capabilities kept track of remotely (col. 7 lines 36-38, 42-52).

17. As per claim 17, Bonola teaches the invention as claimed, including an apparatus comprising:

a plurality of processors coupled to a bus (col. 4 lines 29-33; Fig. 1);

an input/output interface coupled to the bus (col. 4 lines 52-54; Fig. 1);

a plurality of input/output devices coupled to the input/output interface (col. 4 lines 52-57; Fig. 1), the plurality of processors processing program code configured to perform a plurality of tasks (col. 9 lines 24-27), the program code comprising:

program code configured to cause a first portion of the plurality of processors to interact with a first input/output device of the plurality of input/output devices (col. 7 lines 22-25);

program code configured to cause a second portion of the plurality of processors to interact with a second input/output device of the plurality of input/output devices (col. 7 lines 42-52);

program code configured to cause a second portion of the plurality of processors to emulate a specific microprocessor instruction set (col. 8 lines 11-18);

wherein the first portion of the plurality of processors provides functionality as found in a first application-specific subsystem and wherein the first input/output device is the first application-specific subsystem (col. 3 lines 23-30); and

wherein the second portion of the plurality of processors provides functionality as found in a second application-specific subsystem and wherein the second input/output device is the second application-specific subsystem (col. 7 lines 42-52; col. 8 lines 11-18).

18. As per claim 14, Bonola teaches the invention as claimed, including the apparatus of claim 17 further comprising:

kernel program code configured to dynamically allocate the processing of the program code among the plurality of processors (col. 3 lines 26-35; col. 7 lines 22-33; col. 8 lines 11-18).

Response to Arguments

19. **Applicant's arguments filed August 5, 2005 have been fully considered but they are not persuasive.**

20. Applicant contends that the structure of the claimed invention is distinct from Bonola, in that "*Bonola does not appear to teach a homogenous processing system since if it was homogeneous, all of the processors could process the commands and there would not be a need for another processor to process a mismatched command.*"

21. This argument incorrectly characterizes Bonola. Even if it were accepted as true, it would indicate that the claimed invention is not a homogenous processing system either. If a processor being configured to perform a particular function makes a system heterogeneous, the claimed invention would be directed to a heterogeneous set of processors, since the processors therein are described as emulating different instruction sets and performing different types of

processing. Regardless, the argument mischaracterizes Bonola, as it is explicitly stated that the processors are identical (col. 4 lines 43-47, "the CPUs...are essentially identical in configuration and function"), just as Applicant's specification indicates the claimed plurality of processors are identical, i.e. homogeneous (pg. 4, "General purpose processors...are substantially identical).

22. Applicant argues that the claims are distinct from Bonola based on the new limitations in the independent claims directed to performance of "*graphics image processing, video processing and audio processing and communications processing.*"

23. However, these features are merely a recitation of the intended use of the claimed invention. Such an intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. By loading a processor with the information necessary to proceed with processing of a particular task, the processors may perform any of graphics image processing, video processing, audio processing, or communications processing.

24. Applicant argues that Bonola fails to teach "*interacting with first...and second input/output devices by the multiple processors [or]... causing a second portion of the plurality of processors to emulate a specific microprocessor instruction set.*"

25. Examiner respectfully disagrees. Concerning the alleged failure to disclose interacting with input/output devices, attention is directed to Fig. 1 of Bonola. The plurality of processors 20-23 communicate with input output devices 62, 68, 71, etc. over a plurality of buses 24, 42,

and 60. One of ordinary skill in the art would recognize that based on the computer configuration depicted in Fig. 1, the plurality of processors inherently are in communication with every input/output device attached to the computer. Regarding the alleged failure to teach emulation, the teaching in Bonola directed to loading the slave processor with all the necessary information to process a specific type of command is emulation (col. 3 lines 37-44). In fact, Bonola specifically indicates that if the slave processor is unable to perform the task, the host processor will perform the emulation (col. 3 lines 26-35).

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed J. Ali whose telephone number is (571) 272-3769. The examiner can normally be reached on Mon-Fri 8-5:30, 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai T. An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Syed Ali
October 14, 2005

MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100